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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/643,799	08/18/2003	Shao-Po Wu	APRI-P013	7472

758 7590 08/05/2005

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EXAMINER
DOAN, NGHIA M

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SP

Office Action Summary	Application No.	Applicant(s)	
	10/643,799	WU ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08/18/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/18/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application filed on 80/18/2003, claims 1-20 are pending.

Drawings

2. The drawings are objected to because **the figure 1 and figure 3 are not shown the inputs came from where and the destination of the outputs. The figure 2 shows numbers 21 and 22 are same element**. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 1 is objected to because of the following informalities: **the claim 1 contains a term " may be" before "executed independently", the term " may be" is not a definite language.**

Term "**the**" before "second modified circuit" is should be written -- **a** --

Based on the abstract and specification, the examiner suggest that the preamble of claim 1 should be rewritten as **"A system for design verification and manufacturing enhancement comprising:"**.

Appropriate correction is required.

4. Claims 2, 5, 6, 13 are objected to because of the following informalities: (claim 2, and 13) contain "a storage repository", (claim 5) contains "first and second processors", and (claim 6) contains "layout sub-divisions", these limitations are not disclosed by the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1-13 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 contains the limitations such as **"first**

enhancement portion", " first modified circuit", "second enhancement portion", "second modified circuit" and "tag", these elements have not been described in the specification. Since claims 2-13 all depend directly or indirectly on claim1, they contain the limitations of claim 1 and therefore are also rejected.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kochpathcharin et al. (Kochpathcharin) (US 2004/0181769).

9. **With respect to claim 1**, Kochpathcharin discloses a system for design verification and manufacturing enhancement (fig. 4) comprising:

a first enhancement portion for verifying or enhancing a circuit definition to generate a first modified circuit definition with at least one tag (applicant has not specifically defined what he/her means by " first enhancement portion", "first modified circuit", and "tag" are also not indicated in any drawing). Examiner is therefore broadly reading **"first enhancement portion"** in claim as **"application 1 CS1"; " first modified circuit",** in claim as **"customer reticle set";** and **"tag"** in claim as **"Device ID".** With this in mind the above claimed that a first enhancement portion (application 1 CS1) for verifying or enhancing a circuit definition to generate (receive) a first modified

circuit definition (customer reticle set) with at least one tag (device ID) (fig. 4, pg. 2, ¶ 33, ll. 3-4; fig. 7A-7F)

, and Examiner is also broadly reading that a "**second enhancement portion**" in claim as **"Application 2 CS4";** and **"second modified circuit"** in claim as "**foundry reticle set**". With this in mind the above claimed that a second enhancement portion (Application 2 CS4) for verifying and enhancing a second modified circuit definition (foundry reticle set) (fig. 4, pg. 2, ¶ 33, ll. 3-4), wherein:

the first modified circuit definition (customer reticle set) and the second modified circuit definitions (foundry reticle set) (pg. 2, ¶ 30, ll. 2-5, ¶ 33, ll. 3-4) comprise:

one or more geometry representations (pg. 3, ¶ 51 and ¶ 54), and

one or more placement rules (pg. 2, ¶ 34 and pg. 2, ¶ 93);

further comprising an interface (internet) between said first enhancement portion (application 1 CS1) and said second enhancement portion (Application 2 CS4), such that said first enhancement portion and said second enhancement portion may be executed (operated/run) independently (fig. 4, pg. 5, ¶ 111-113).

10. **With respect to claims 2 and 13**, Kochpathcharin discloses the system in claim1, further comprising:

(claim 2) a storage repository (master repository) (fig. 6) for storing said first enhancement and said second enhancement and storing one or more circuit design rules (design rules), one or more circuit design goals (purpose) and one or more manufacturing specific geometry rules (pg. 7, ¶ 145, 155-160, and 161).

(claim 13) wherein storage repository comprises: a volatile portion and non-volatile portion (fig. 6, pg. 5, ¶107, ll. 7-11).

11. **With respect to claim 3**, Kochpathcharin discloses the system in claim1, further comprising:

a modification interface for modifying the first enhancement and modifying the second enhancement, and wherein the output of said second modified circuit definition at least the structure is modified according to said manufacturing specific geometry rules (abstract, fig. 6, pg. 1, ¶ 9-16).

12. **With respect to claim 4**, Kochpathcharin discloses the system of claim 1 further comprising: a data mapper which translates (conversion) between said circuit definition (layout information) and said geometry representations (foundry format or mask writer format) (pg. 2, ¶ 31, ll. 6-9, and ¶ 35).

13. **With respect to claim 5**, Kochpathcharin discloses the system of claim 1 further comprising: a hierarchical data partitioner for enabling distributed processing by one portion in a processor and a second portion in a second processor (fig. 4, pg. 5, ¶95, ll. 4-7).

14. **With respect to claim 6**, Kochpathcharin discloses the system of claim 1 further comprising: said hierarchical data partitioner enables a merging of a plurality of independent layout sub-divisions (array) (pg. 3, ¶54, ll. 10-14, pg. 4, ¶ 96).

15. **With respect to claim 7**, Kochpathcharin discloses the system of claim 1 further comprising: said manufacturing-specific geometry rules comprise one or more manufacturing process models, or one or more layout enhancement methodologies (fig. 5).

16. **With respect to claims 8-10**, Kochpathcharin discloses the system of claim 1 further comprising: said one or more circuit design rules and said one or more circuit

design goals and said one or more manufacturing-specific geometry rules use a common user interface (fig. 5, fig. 6).

(claim 9) said circuit design rules, said circuit design goals and said manufacturing-specific geometry rules comprise circuit nets, circuit functions, circuit timing requirements, circuit delay characteristics, the circuit layout and manufacturing-specific process rules (¶ 145-167).

(claim 10) said manufacturing-specific process rules use a process rule design chip fabricated by a manufacturer governed by said manufacturing-specific geometry rules. (¶ 145-167).

17. **With respect to claim 11**, Kochpathcharin discloses the system of claim 1 further comprising: said circuit definition comprises a portion of a larger circuit (inherent in fig. 5).

18. **With respect to claim 12**, Kochpathcharin discloses the system of claim 1 further comprising: said circuit definition comprises one or more circuit and layout files in GDSII format (fig. 1, fig. 2A, and 2B).

19. **With respect to claim 14**, Kochpathcharin discloses an integrated design verification and manufacturing enhancement tool comprising:

a physical verification and enhancement platform (application1 CS1) with an interface to at least one other verification or enhancement engine (application 2 CS4, application 1 CS2 -- Mask Shop--) (fig. 4) , and

a common data structure for at least one layout geometry or circuit connectivity engines (pg. 4, ¶ 79; pg. 6, ¶ 128), and

wherein said platform rule checking for geometric or connectivity operations can be executed sequentially or iteratively (fig. 2A, 2B, step 240, 250; pg. 4, ¶ 79, 83 and 83).

20. **With respect to claims 15 and 16,** Kochpathcharin discloses the tools in claim 1, (claim 14) wherein said data structure comprises: a representation of polygons (pg. 3, ¶ 54), wherein: said polygon has a set of vertices and a plurality of pointers associated with other polygons (pg. 3, ¶ 54).

(claim 16) said polygon vertices represent a shape and location of said polygon (pg. 3, ¶ 96).

21. **With respect to claim 17,** Kochpathcharin discloses the tools in claim 1, (claim 14) wherein said interfaces operate according to a common command script (fig. 4).

22. **With respect to claims 18 and 19,** Kochpathcharin discloses the tools in claim 1, (claim 18) wherein said interfaces comprise a graphical user interface to display data or process flow in a plurality of stages of the physical verification or enhancement process (fig. 5, fig. 7A-7F).

(claim 19) said interfaces comprise a circuit and layout editor which interactively displays a process flow in one or more stages of the physical verification or enhancement process and enables changing of input data (fig. 1, 2A, 2B, 5, and 7A-7F).

23. **With respect to claim 20**, Kochpathcharin discloses a method for mask set generation comprising the steps of:

receiving a physical design file comprising the output from an integrated design verification and manufacturability enhancement tool (fig. 1, step 140A, pg. 4, ¶ 79), and

generating a mask set using said physical design file to fabricate an integrated circuit (fig. 1, step 140A, pg. 4, ¶41).

24. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

25. Claims 14-16 is rejected under 35 U.S.C. 102(b) as being anticipated by DeCamp et al. (DeCamp) (US 6,063,132).

26. **With respect to claim 14, DeCamp** discloses an integrated design verification and manufacturability enhancement tool (software) (DeCamp) abstract), comprising:

a physical verification and enhancement platform (SHAPEDIFF) (co. 5, ll. 2-9) with an interface to at least one other verification or enhancement engine (runset file and testcase file) (Decamp, col.3, ll. 1-5; ll. 11-21), and

a common data structure for at least one layout geometry or circuit connectivity engines (Decamp, col. 2, ll.13-22), and

wherein said platform rule checking for geometric or connectivity operations can be executed sequentially or iteratively (Decamp, col. 5, ll. 47-64).

27. **With respect to claims 15 and 16, DeCamp** discloses the tools in claim 1, (claim 14) wherein said data structure (boundary shape) (Decamp, col. 6, ll. 1-3) comprises:

a representation of polygons (least-enclosing polygon) (Decamp, col. 6, ll. 6-10) wherein:

said polygon has a set of vertices and a plurality of pointers (mapping) associated with other polygons (Decamp, col. 6, ll. 52-65).

(claim 16) said polygon vertices represent a shape and location of said polygon (Decamp, col. 6, ll. 10-17).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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